

## REMARKS

The enclosed is responsive to the Examiner's Office Action mailed on September 12, 2005. At the time the Examiner mailed the Office Action claims 1-43 were pending. By way of the present response the Applicants present arguments in response, and make no amendments to the claims. As such, claims 1-43 are now pending. The Applicants respectfully request reconsideration of the present application and the allowance of all claims now presented.

### Drawing Rejections

Figures 1-2 have been amended and designated by a legend such as Prior Art.

### Claim Rejections

#### 35 U.S.C. 103(a) Rejections

The Examiner rejected claims 1-43 under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) as described in the background of the invention [specification pages 1-2 and figures 1-2].

Applicant respectfully asserts that the cited references fail to teach or render obvious Applicant's invention as claimed in claims 1-43. First, the Examiner has impermissibly relied on common knowledge in the art in rejecting claims 1-43. Second, the common knowledge mistakenly relied upon has been mischaracterized by the Examiner, and therefore even if it can be unquestionably

demonstrated to be common knowledge, it still does not teach or render obvious Applicant's invention as claimed in claims 1-43. Finally, the Examiner has not met his burden of proof for a *prima facie* case of obviousness because there is no suggestion or motivation to combine references, and the cited prior art does not teach or suggest all of the claim limitations of claims 1-43.

### 1. Impermissible Reliance on Common Knowledge in the Art

First, the Examiner has impermissibly relied on common knowledge in the art in rejecting claims 1-43. The Examiner has relied on common knowledge for two purposes: 1) to show that the second addressable device includes a circuit to generate a second device ID as a function of the first device ID; and 2) to show a motivation to combine the common knowledge with the admitted prior art.

Official notice without documentary evidence to support an examiner's conclusion is permissible only in some circumstances. (MPEP 2144.03(A)) Official notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known. (MPEP 2144.03(A)) It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration of being well-known. (MPEP 2144.03(A))

Applicant asserts that it is not well known in the art that adjacent memory locations or entries always have an address or identification that is linearly

related to the current location or entry. Applicant further asserts that it is not well known in the art to generate an address or pointer value associated with a next memory location or entry by adding or subtracting the current memory address or pointer value by a constant. Applicant believes that these are not well known in the art because the claimed invention relates to physical stacking of multiple addressable devices, where a device identifier for a second device is generated as a function of the device identifier of a first device.

## 2. "Common Knowledge" Mischaracterized by the Examiner: Not Analogous Art

Second, the common knowledge mistakenly relied upon has been mischaracterized by the Examiner, and therefore even if it can be unquestionably demonstrated to be common knowledge, it still does not teach or render obvious Applicant's invention.

Applicant has claimed in claim 1: "An apparatus comprising: a first addressable device associated with a first device identifier (ID); a second addressable device stacked adjacent the first addressable device, wherein the second addressable device is coupled to the first addressable device and includes a circuit to generate a second device ID as a function of the first device ID."

The "well-known" art taken notice of by the Examiner relates to memory stacks and stack pointers. Applicant's understanding of the Examiner's characterization is that the "memory stacks" and "stack memories" referred to by the Examiner are related to the way memory is allocated and/or accessed during

program execution. However, this is unclear, as the Examiner has not cited any specific references to illustrate what is “known and widely practiced in the pertinent art.”

Assuming that the Examiner is indeed referring to memory stacks in a computer programming and/or memory usage sense, this type of memory stack is quite different from a stack as defined in the present application. As illustrated in Figure 4, a “stack” as used in the present application includes multiple physical addressable devices, such as memory devices, which are physically stacked on/adjacent to one another in a package. For example, refer to Figure 4, where multiple physical die (410, 412, 414, 416) are physically stacked together in a package (400).

To rely on a reference under 35 USC 103, it must be analogous prior art. (MPEP 2141.01(a)) In order to rely on a reference as a basis for rejection of an applicant’s invention, the reference must either be in the field of applicant’s endeavor, or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned. (MPEP 2141.01(a)) A “memory stack” in a computer programming sense is not in the same field of endeavor as physical stacking of memory devices in a package. Furthermore, the problem addressed in this application is the existence of bond wires 116 (Fig. 1) for generating device IDs. Use of bond wires may cause problems related to manufacturing complexity and/or reliability, and may present other issues as well. Applicant’s claimed invention aims to solve these potential problems by eliminating the bond wires, and instead using a “circuit to generate a second device ID as a function

of the first device ID." Memory stacks in a computer programming sense are not reasonably pertinent to this problem.

Because a "memory stack" in a computer programming sense is not analogous to a physical stack of multiple addressable devices in a single package, it may not be used in rejecting claims 1-43 under 35 USC 103.

### 3. Burden of Proof Not Met for Prima Facie Case of Obviousness

Finally, the Examiner has not met his burden of proof for a *prima facie* case of obviousness because even if the commonly known art cited by the Examiner is valid art for the purposes of a 35 USC 103 rejection, there is no suggestion or motivation to combine references, and the cited prior art does not teach or suggest all of the claim limitations. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references) must teach or suggest all of the claim limitations. (MPEP 2143)

The Examiner stated: "One having ordinary skill in the art... [who] looks at the teaching of the prior art, would leads [sic] he or she to further employ the commonly used logic for generating a second memory device ID by adding or subtracting the current ID." Assuming arguendo that the statements made by the Examiner are valid prior art to employ in a 35 USC 103 rejection, the fact that the

claimed invention is within the capabilities of one of ordinary skill in the art is not sufficient by itself to establish *prima facie* obviousness. (MPEP 2143.01)

The Examiner also states that "It would have been obvious because memory units in a stacked memory device are identified in the same manner as stacked entries in a stack memory." Applicant believes that this is an untrue statement, because memory units in a stacked memory device are not analogous to stacked entries in a stacked memory for the reasons described above. Therefore, this reasoning does not set forth a suggestion or motivation to combine the references.

Finally, the prior art references do not teach or suggest all claim limitations, as required to establish a *prima facie* case of obviousness. The Examiner has not set forth any specific prior art reference that teaches "a second addressable device ... including a circuit to generate a second device ID as a function of a first device ID." The admitted prior art relates only to hard wiring of device IDs. There is no valid prior art reference cited that relates to generation of device IDs in any manner other than by hard wiring.

Therefore, the Examiner has not met the required burden of proof for setting forth a *prima facie* case of obviousness for claims 1-43.

In light of the comments above, the Applicant respectfully requests the withdrawal of the 103 rejection and allowance of claims 1-43.

## CONCLUSION

Applicant respectfully submits that the 35 USC 103(a) rejection of claims 1-43 has been overcome and that all pending claims are in condition for allowance.

If there are any additional charges, please charge them to our Deposit Account Number 02-2666. If a telephone conference would facilitate the prosecution of this application, the Examiner is invited to contact Thomas C. Webster at (408) 720-8300.

Respectfully Submitted,  
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 12/15, 2005

  
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**Amendments to the Drawings:**

The attached sheet of drawings includes changes to Figures 1 and 2. These figures replace the original Figures 1 and 2. In Figures 1 and 2 the legend Prior Art has been added.

Attachment:                    Replacement Sheet